In the Claims:

Please amend the claims as follows:

1. (Currently Amended) A non-volatile memory cell integrated on a semiconductor substrate and comprising:

a floating gate transistor including a source region and a drain region, a gate region projecting from the substrate and comprised between said source and drain regions, said gate region having a predetermined length and width and comprising a first floating gate region and a control gate region, ~~characterised in that~~ wherein said floating gate region is insulated laterally, along the width direction, by a dielectric layer with low dielectric constant value.

2. (Currently Amended) A memory cell according to claim 1, ~~characterised in that~~wherein said floating gate regions are covered by a dielectric layer before being insulated from each other through said dielectric layer with low dielectric constant value.

3. (Currently Amended) A memory cell according to claim 1, ~~characterised in that~~wherein said dielectric layer with low dielectric constant value is bounded between said floating gate regions.

4. (Currently Amended) A memory cell according to claim 1, ~~characterised in that~~wherein said dielectric layer with low dielectric constant value is formed by a layer of material having a dielectric constant comprised between 1 and 3.9.

5. (Currently Amended) A memory cell according to claim 1, ~~characterised in that~~wherein said dielectric layer with low dielectric constant value is formed by a silicon oxide layer doped ~~for example~~ with fluorine.

6. (Original) A memory cell according to claim 1, ~~characterised in that~~wherein said dielectric layer with low dielectric constant value is formed by a carbon oxide layer hydrated

with alkylic groups.

7-14. (Cancelled)

15. (Currently Amended) A memory cell matrix formed on a semiconductor substrate comprising a plurality of memory cells organized in rows and columns, each cell being formed according to claim 1, the cell matrix being ~~characterised in that~~wherein adjacent memory cells belonging to a same row of said memory cell matrix are insulated from each other by a dielectric layer with low dielectric constant value.

16. (Original) A memory-cell structure formed on a semiconductor substrate, the memory-cell structure comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell structure including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the structure.

17. (Original) The memory-cell structure of claim 16 further comprising a dielectric layer having a greater dielectric constant than the insulating regions formed on the floating gate regions.

18. (Original) The memory-cell structure of claim 16 wherein the insulating layer has a dielectric constant having a value of between approximately 1 and approximately 3.9.

19. (Original) The memory-cell structure of claim 16 each memory cell further comprises a control gate region capacitively coupled to the floating gate region through a dielectric layer having a dielectric constant greater than that of the insulating layer, and wherein the control gate regions of memory cells in respective rows are electrically interconnected.

20. (Original) The memory-cell structure of claim 16 wherein each memory cell comprises a FLASH memory cell.

21. (Original) A memory device, comprising:

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the array.

22. (Original) The memory device of claim 21 wherein the memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell.

23. (Original) The memory device of claim 21 further comprising a dielectric layer having a greater dielectric constant than the insulating regions formed on the floating gate regions.

24. (Original) An electronic system, comprising:

a memory device including,

a memory-cell array formed on a semiconductor substrate, the memory-cell array comprising a plurality of non-volatile memory cells arranged in rows and columns and formed on the semiconductor substrate, each memory cell including a floating gate region and the memory-cell array including an insulating region having a relatively low dielectric constant formed between adjacent floating gate regions of memory cells in respective rows of the array.

25. (Original) The electronic system of claim 24 wherein the electronic system comprises a computer system.

26. (Original) The electronic system of claim 25 wherein the memory device comprises a FLASH memory device and each memory cell comprises a FLASH memory cell.

27-30. (Cancelled)